REMARKS

At the time of the Examiner's Action, claims 1-9 were pending in the application, claims 10-18 being previously cancelled on July 11, 2003 in a response to a restriction requirement. As a result of this Amendment, original claims 1-9 remain.

The Examiner rejected Claims 1-3 and 6-9 under 35 U.S.C. §102(b) as being anticipated by Hartmann (US Patent No. 6,096,091, hereinafter "Hartmann").

The Examiner rejected Claims 4-5 under 35 U.S.C. §103(a) as being unpatentable over Hartmann in view of Cooke et al (U.S. Patent No. 5,970,254, hereinafter "Cooke").

Regarding Hartmann, although this reference might appear similar to the claimed invention at first blush, the purpose and teaching of Hartmann is quite different from the teaching and scope of the claimed invention. Hartmann discusses reconfigurable logic networks that are interconnected by buffering to isolate the logic networks from timing and clocking problems which slow or limit daisy chaining of dynamically reconfigurable logic. Hartmann enables runtime or "on-the-fly" reconfiguration of one or more the logic networks while attempting to avoid the aforementioned timing and clocking problems.

In contrast, the present invention is directed towards customization of an FPGA-based SoC by selecting system components and configuring such components with parameters that are propagated to peer system components during customization rather than the runtime reconfiguration taught by Hartmann. Note that the purpose of the present invention is quite different from the purposes discussed in Hartmann. As mentioned in the specification of the present invention, customization is typically constrained by the availability of FPGA-based SoC resources. These resources can be LUTs, slices, BRAMS, D-Flip flops, memory and processing power among other things. Instead of isolation as taught in Hartmann, the customization performed

is done with a view of the whole FPGA-based SoC where exemplary system and parameter consistency checks can include, matching data bus widths of peripherals and system components, determining interrupt conflicts, determining memory map conflicts, determining memory size and usage, determining device counts, determining availability of FPGA resources and determining maximum operating frequency. In this regard, there is no propagation of parameters among peer system components in Hartmann. Instead, individual reconfigurable logic networks 120A and 120B in Hartmann are individually programmed using an embedded processor and a logic configuration library 160. The networks 120A and 120B remain isolated using buffers. As described in Hartman, Col. 4, lines 30-45, each logic network operates on a separate clock and the buffers isolate each of the reconfigurable logic networks. Hartmann is not a system that propagates parameters as claimed in the present invention, but rather isolates logic networks using buffers to overcome its timing problems. Hartmann does not propagate configurations and parameters from one logic network to another. Instead, each configuration is stored in the library 160 and each logic network is programmed individually without the propagation of parameters from one system component to another.

Further note that the present invention also configures selected system components with parameters used to configure peer components as in claim 2 and furthermore propagates parameters used to configure peer components to subsequently selected system components used to configure the FPGA-based SoC as in claim 3.

Thus, Applicant respectfully believes Hartmann fails to anticipate claims 1-3 and 6-9 of the present invention and that the existing claims overcome the rejection under 35 U.S.C. §102(b). Furthermore, it is suggested that Hartmann even teaches away from the claims of the present invention due to its emphasis on isolation between the individual logic networks.

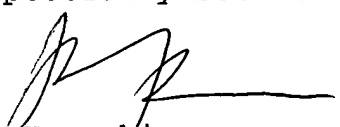
Regarding Cooke and the rejection of claims 4 and 5, Cooke does discuss the use of software tools to recompile application code into a combination of software and reloadable hardware blocks. Nonetheless, Cooke fails to discuss the selection of a hardware core or a software core (such as an IP core). Nor is there any teaching, suggestion, or mention in Cooke or in Hartmann individually or in combination of configuring a system component (such as a hardware core or a software core) during customization of an FPGA-based SoC with parameters that can be propagated to peer system components as claimed. Furthermore, as previously noted, it is believed that Hartmann teaches away from the claims of the present invention due to its emphasis on isolation between the individual logic networks. Thus, Applicant respectfully believes that Hartmann in view of Cooke fails to obviate claims 4 and 5 of the present invention and that existing claims 4 and 5 overcome the rejection under 35 U.S.C. §103(a).

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,



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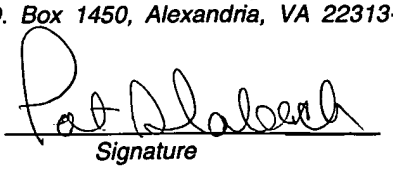
*Name* Pat Slaback _____ 

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